Layout Optimizations for THz Integrated Circuit Design in Bulk Nanometer CMOS

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***Abstract*—Scaling in CMOS has increased the attainable operational frequencies, while greatly increasing the transistor's parasitic modeling complexity. Additionally, the performance of the ever-smaller on-chip passives for mm-wave and THz circuits is being degraded by numerous process requirements and limitations, such as high densities of dummy metals. This work discusses the main transistor layout trade-offs for high-frequency performance in both 40nm and 28nm bulk CMOS. The impact of dummy metals on a single-turn on-chip inductor for mm-wave/THz frequencies is presented, which shows that low dummy metal densities around critical high-frequency passives are essential to minimize degradation in performance.**

***Index Terms*—THz, CMOS, harmonics, transistor fmax, dummy fill**

I. Introduction

The reduction of CMOS transistor gate length in nanometer CMOS technology nodes enables integrated circuits operating at ever higher frequencies. Due to the limited f_{max}, fundamental THz circuits are not possible in current CMOS nodes. By utilizing near-f_{max} circuits for harmonics generation, (sub-) THz signals can be generated above f_{max} in CMOS [1]. The evolution of both f_t and f_{max} is predicted by the International Technology Road-map for Semiconductors (ITRS), and the improvement with scaling is illustrated in Fig. 1. While the predicted values of the f_t remain consistent over the years of reporting, the accuracy of the f_{max} road-map is definitely lower as reflected by the shifting values with each report. This can be attributed to the rising number of parasitic effects in deep sub-micron technologies, which makes designing circuits operating close to the technology's f_{max} more and more complex.

This work aims to discuss some of the issues and optimizations when designing and layouting both actives and passives for THz CMOS circuits. As the low-frequency models of these components are no longer valid at mm-wave and higher frequencies, more attention has to be spend in modern nanometer CMOS processes on optimizing the transistor layout (Section II) and to minimize the impact of ever stricter process requirements on passives (Section III).

II. CMOS transistor optimization

A. f_{max} performance of individual transistor

The f_{max} of a transistor is a good measure for its high-frequency performance. It is the frequency where the power gain of the device reaches unity, and is strongly dependent on the layout of the transistor (Eq. 1). The dominant layout factor determining the f_{max} is the gate resistance R_g, which can be minimized by placing many narrow fingers with gate contacts on both sides of the transistor. However, the width of the fingers cannot be reduced indefinitely, as for very narrow and short fingers, the increasing routing network and resulting parasitic capacitance and resistance become dominant.

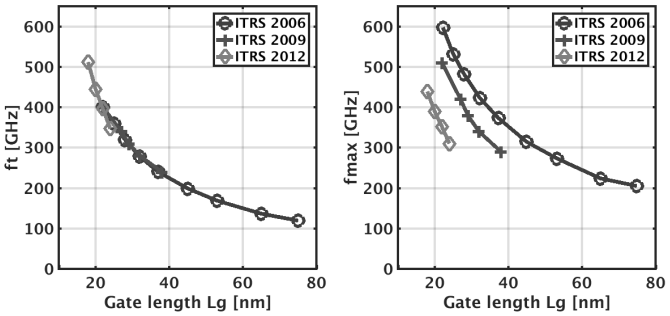


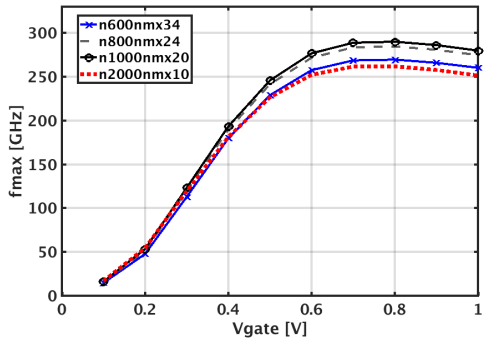
Fig. 1: Evolution of the ITRS roadmap predictions for f_t and f_{max} for decreasing transistor length

$$f_{max} = \frac{f_t}{2 \cdot \sqrt{[g_{ds} \cdot (R_g + R_s + r_{ch}) + 2 \cdot \pi \cdot R_g \cdot C_{gd}]}} \quad (1)$$

This optimum in transistor finger width can be seen when evaluating the simulated f_{max} for a $20\mu m/40nm$ NMOS in a 40nm CMOS process (Fig. 2a). A finger width of $\approx 1\mu m$ results in a trade-off between the gate resistance R_g and added parasitics of the metal traces connecting all the gate fingers. For a 28nm CMOS process, however, this trade-off is not there: reducing the finger width keeps increasing the f_{max} (Fig. 2b). The large number of gate fingers will require more interconnection, but the losses introduced by this larger routing network do not outweigh the benefit of reducing R_g, which remains the dominating factor. For the optimal high-frequency performance in 28nm CMOS, the finger width should be reduced down to the minimal width allowed by the process.

B. Cross-coupled pair and generating negative resistance at the edge of technology

When utilizing harmonics to generate THz signals, the below-f_{max} fundamental oscillator (ex. cross-coupled LC VCO) will require transistors operating at the edge of their high-frequency capabilities. While f_{max} is a useful metric to determine the high-frequency potential of a design, ultimately



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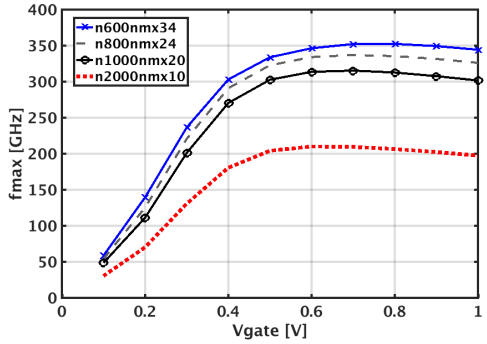
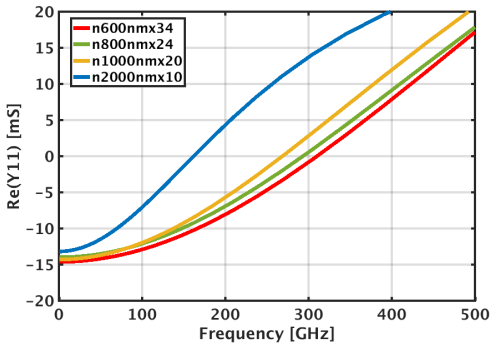


(b)

Fig. 2: Influence of W on f_{max} (simulated), comparison between (a) 40nm and (b) 28nm CMOS



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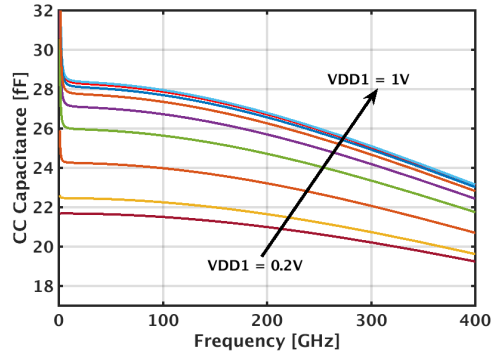


(b)

Fig. 3: Negative resistance (a) and parasitic capacitance (b) generated by a 28nm CMOS cross-coupled transistor pair

the purpose of the cross-coupled transistor pair is to generate a negative resistance to compensate for the losses of the LC resonator tank. Fig. 3 shows the real part of $Y_{cross-coupled}$ for different cross-coupled ultra-low V_t (ULVT) transistor finger widths ($F = 20\mu m$) implemented in a 28nm CMOS process. The frequency where the negative resistance crosses from negative to positive is f_{gm}, in analogy to the cross-coupled pair sometimes being referred to as 'negative gm'. Similar to the impact on f_{max}, the optimal transistor finger width yields a larger negative resistance up to a higher f_{gm}.

With parasitics becoming a non-negligible part of the transistor, parasitic-aware design approaches can provide useful features. As illustrated in Fig. 3b, changing the supply voltage varies the parasitic capacitance of the cross-coupled pair by a few femto-Farads. When the (fixed) capacitance of the VCO is kept small to enable a higher fundamental oscillation frequency, the influence of this 'parasitic tuning' would allow the omission of additional varactors from the VCO while maintaining frequency tuning capabilities.

III. Impact of Dummy Metals on Passives in Deep-Scale Nanometer CMOS

The scaling of CMOS technology nodes does not only mean that the effective gate length decreases, but also has an impact on the metallization options available to the designer (Fig. 4). The amount of available metal layers has increased to cope with the rising interconnection difficulties that come with the ever-higher density of transistors.

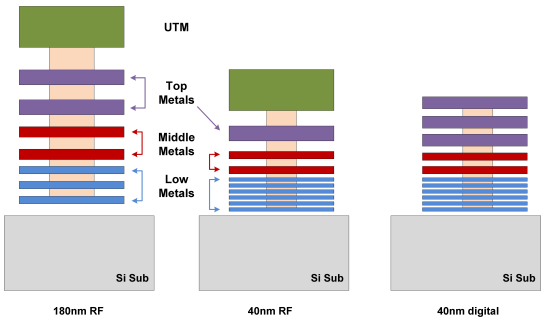
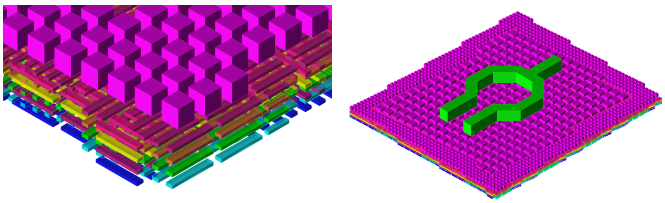


Fig. 4: CMOS metal stack evolution towards deep-scale nanometer nodes

Another major evolution is in the thickness of the different metal layers, and the corresponding proximity to the silicon substrate. The lower layer metal thickness has reduced to very thin traces of $\approx 100nm-200nm$ thin, with a significant rise in the trace sheet resistance. The resistance of vias between metals, especially the lower metals, has also drastically increased for deep-scale nanometer CMOS technologies [2]. While the middle and top metal layer thickness has not changed that immensely over newer technology nodes, the reduction of the

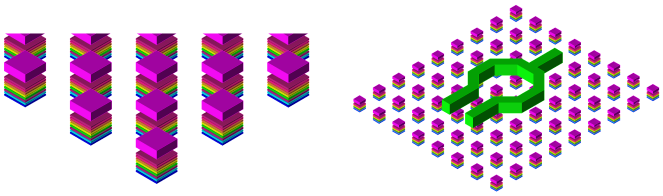
lower metals results in a closer proximity of the higher metals to the lossy substrate.

The importance of metal density rules in deep-scale nanometer CMOS technologies is becoming increasingly important, both production process-wise as for the design of high-frequency passives. When operating at the high-end of the mm-wave spectrum, passives become very small and the presence of nearby dummy metals has an increasing impact on the passives performance. The impact of dummy metals on transformers and inductors up to 60GHz has already shown that for mm-wave frequencies, there is a noticeable influence [3]–[5]. In the following section, this work presents the impact of dummy metals on on-chip inductors used in THz circuits.



(a) (b)

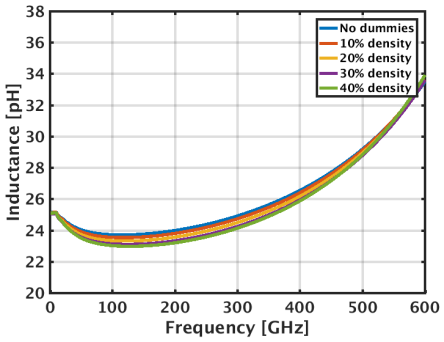
Fig. 5: Close-up of dummy metals (a) and a single-turn on-chip inductor with surrounding dummy metals (b), both generated by an automatic filling tool



(a) (b)

Fig. 6: Close-up of dummy metals (a) and a single-turn on-chip inductor with a 10% dummy metal density (b), manually placed

The foundry-provided dummy filling tool aims to generate a 80-90 percent metal density, and yields a dummy-filled layout as depicted in Fig. 5. While this high, uniform metal density is good to minimize any process-related variations, it is virtually impossible to simulate due to the dense mesh of very narrow metal strips. To analyze the impact of different dummy metal densities at (sub-)mm-wave frequencies, a fixed dimension dummy unit structure is manually placed to achieve 10 to 40 percent metal density (as shown in Fig. 6) around an inductor with $15\mu m$ inner diameter and $5\mu m$ trace width. Each unit dummy structure consists of metal square of all consecutive dummy metals. The structures are spaced evenly to achieve the desired density, and the inductor is implemented in the top UTM layer and simulated in a 2.5D EM simulator (ADS Momentum). Using $2.4\mu m$ x $2.4\mu m$ squares allows relatively fast simulations while maintaining high simulation accuracy.



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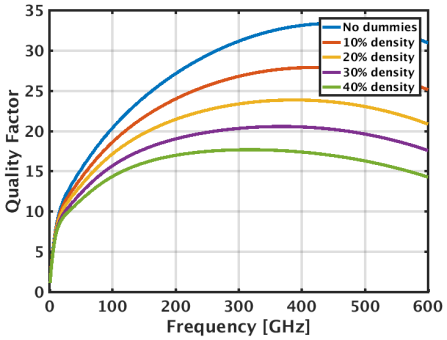


(b)

Fig. 7: Simulated inductor inductance (a) and quality factor (b) of a top-metal single-turn inductor with varying density of manually placed dummy metals

The resulting simulated inductance L and inductor quality factor Q for different dummy metal densities are shown in Fig. 7. While the inductance does not vary greatly, an extensive divergence is seen when looking at the quality factors of the various metal densities: the difference in quality factor with and without dummies increases at higher frequencies. At RF frequencies, the impact of the dummy metals is minimal, while a noticeable difference is detectable at mm-wave frequencies. The spread in quality factor between 0% and 40% dummy fill is 25% at 80GHz, while at 200GHz, adding 40% of dummies decreases the total quality factor by half compared to the same, dummy-free inductor.

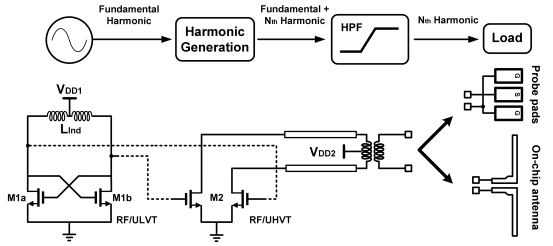
The dominant loss mechanisms due to dummy filling are the magnetically induced eddy currents in the dummy metal structures and the additional capacitive coupling to the lossy silicon substrate. At low frequency (10GHz), the losses of the inductor are dominated by the resistive losses of the metal inductor trace and the eddy currents in the dummy metals are minimal. At mm-wave frequencies (60GHz), the magnetic field of the inductor starts to induce observable eddy currents in the top layers of the dummy structure. From this point on in the frequency spectrum, the dummies start to have a substantial impact on the quality factor of the inductor. At higher frequen-

cies (200GHz and 300GHz), the dummy structure becomes a capacitive path to the substrate, further increasing the total parasitic capacitance to the substrate and lowering the self-resonance frequency of the inductor (993GHz/936GHz for 0%/40% dummies). The losses are now both the eddy currents being induced in all metal layers of the dummy structure, as well as the increased coupling to the lossy silicon substrate. To verify that a major part of the losses is due to the presence of metal dummies themselves and not because of coupling to the substrate, an inductor without substrate and 0%/30% dummies is simulated. The difference in inductance between the two cases remains small, while the quality factor drops with almost a third at 200GHz due to eddy currents.

Clearly, this shows that dummy metals have a significant impact on the behavior of mm-wave and certainly THz passives.

IV. Implementation of THz signal generators in bulk nanometer CMOS

Using the above-mentioned approaches, harmonic THz signal sources are implemented in 40nm and 28nm bulk CMOS. The circuit topology is shown in Fig. 8a. The signal generation starts with a LC-VCO with cross-coupled transistors to generate the fundamental frequency. The VCO is connected to a differential amplifier, which generates the third harmonic while also acting as a buffer between the output and the VCO core. This third harmonic is then coupled through a transformer to the output load, being a probe pad or antenna.



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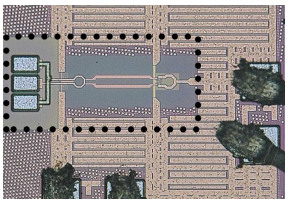

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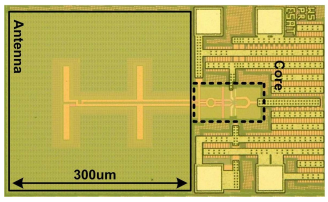
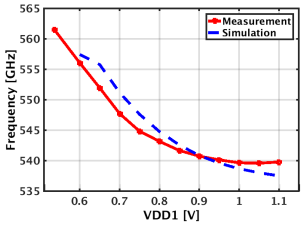


(c)

Fig. 8: Schematic and die photographs of a 0.54THz and 0.6THz transmitter in resp. 40nm and 28nm bulk CMOS

A 0.54THz source [1] is implemented in 40nm CMOS (Fig. 8b), with a 539-561GHz tuning range thanks to 'parasitic tuning': varying V_{DD1} changes the parasitic capacitance of the core transistors. Frequency and output power measurements fit well with simulations (Fig. 9). Additionally, a 588.9-613.6GHz transmitter with on-chip collinear dipole antenna [6] is fabricated in 28nm CMOS (Fig. 8c), demonstrating the first THz signal generator in 28nm CMOS, despite the increasing parasitic complexity in advanced CMOS technologies [7].



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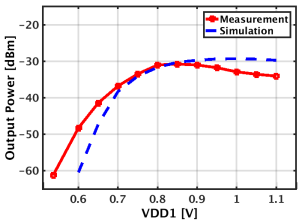

(b)

Fig. 9: Probe measurement results of a 40nm CMOS 0.54THz signal source, showing frequency variation and power fluctuation with varying supply voltage VDD1 [1]

V. Conclusion

The design of THz circuits in CMOS is getting more complicated with scaling due to the increasingly dominant parasitics, the limitations in design freedom and influence of metal density requirements on passives. In this work, a comparison between a 40nm and 28nm CMOS process is made to determine the optimal finger width for highest f_{max} and its ramifications for a cross-coupled VCO. Second, this work presents a study of the influence of dummy metals on a single-turn on-chip inductor designed for harmonics-based THz CMOS circuits. At mm-wave and THz frequency, there is a significant degradation of the inductor quality factor due to surrounding dummy metals. A minimum of dummy metal density should therefore be pursued and manually placed for the critical mm-wave and THz components.

Acknowledgment

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